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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/726,020	11/30/2000	Naoto Abe	862.C1881	1315

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EXAMINER	
LEE, WILSON	
ART UNIT	PAPER NUMBER
2821	

DATE MAILED: 09/11/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/726,020	ABE ET AL.	
	Examiner	Art Unit	
	Wilson Lee	2821	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 November 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *6* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Claim Rejections – 35 USC 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Mitsutake et al. (5,760,538).

Regarding Claim 1, Mitsutake discloses an electron source apparatus (Figure 2) which has an electron source (11-14) and a counter substrate (17) arranged to face the electron source and in which the electron source (11-14) (Col. 7, lines 4-6) has on a substrate (11) a plurality of row-direction wiring line (13), a plurality of column-direction wiring lines (14), insulating layers formed at intersections between the row-direction wiring lines and the column-direction wiring lines (Col. 7, lines 53-55), and a plurality of electron-emitting devices connected to the row-direction wiring lines (13) and the column-direction wiring lines (14) (Col. 7, lines 22-25), and spacer (20) for maintaining an interval between the electron source (12) and the counter substrate (17) (Col. 8, line 65 to Col. 9, line 16 and Col. 27, lines 48-60) is arranged on some of the row-direction wiring lines (13) among the plurality of row-direction wiring lines (13) (Figure 2) characterized by comprising:

a circuit (external circuit or 1702) for sequentially turning on the plurality of row-direction wiring lines (13 or Dx through Dxm) (Figure 18 and Col. 19, lines 50-58); and

a controlled current application circuit (1707) for applying a predetermined controlled current to the plurality of column-direction wiring lines (14 or Dy through Dym) (Figure 18 and Col. 20, lines 46-59).

Regarding Claim 2, Mitsutake discloses an electron source apparatus (Figure 2) which has an electron source (11-14) and a counter substrate (17) arranged to face the electron source and in which the electron source (11-14) (Col. 7, lines 4-6) has on a substrate (11) a plurality of row-direction wiring line (13), a plurality of column-direction wiring lines (14), insulating layers formed at intersections between the row-direction wiring lines and the column-direction wiring lines (Col. 7, lines 53-55), and a plurality of electron-emitting devices connected to the row-direction wiring lines (13) and the column-direction wiring lines (14) (Col. 7, lines 22-25), and spacers (20) for maintaining an interval between the electron source (12) and the counter substrate (17) (Col. 8, line 65 to Col. 9, line 16 and Col. 27, lines 48-60) is arranged on different positions on the plurality of row-direction wiring lines (13) among the plurality of row-direction wiring lines (13) (Figure 2) characterized by comprising:

a circuit (external circuit or 1702) for sequentially turning on the plurality of row-direction wiring lines (13 or Dx through Dxm) (Figure 18 and Col. 19, lines 50-58); and

a controlled current application circuit (1707) for applying a predetermined controlled current to the plurality of column-direction wiring lines (14 or Dy through Dym) (Figure 18 and Col. 20, lines 46-59).

Regarding Claim 3, Mitsutake discloses an electron source apparatus (Figure 2) which has an electron source (11-14) and a counter substrate (17) arranged to face the

electron source and in which the electron source (11-14) (Col. 7, lines 4-6) has on a substrate (11) a plurality of row-direction wiring line (13), a plurality of column-direction wiring lines (14), insulating layers formed at intersections between the row-direction wiring lines and the column-direction wiring lines (Col. 7, lines 53-55), and a plurality of electron-emitting devices connected to the row-direction wiring lines (13) and the column-direction wiring lines (14) (Col. 7, lines 22-25), and spacer (20) for maintaining an interval between the electron source (12) and the counter substrate (17) (Col. 8, line 65 to Col. 9, line 16 and Col. 27, lines 48-60) is electrically connected to some of the row-direction wiring lines (13) among the plurality of row-direction wiring lines (13) (Figure 2) characterized by comprising:

a circuit (external circuit or 1702) for sequentially turning on the plurality of row-direction wiring lines (13 or Dx through Dxm) (Figure 18 and Col. 19, lines 50-58); and

a controlled current application circuit (1707) for applying a predetermined controlled current to the plurality of column-direction wiring lines (14 or Dy through Dym) (Figure 18 and Col. 20, lines 46-59).

Regarding Claim 4, Mitsutake discloses an electron source apparatus (Figure 2) which has an electron source (11-14) and a counter substrate (17) arranged to face the electron source and in which the electron source (11-14) (Col. 7, lines 4-6) has on a substrate (11) a plurality of row-direction wiring line (13), a plurality of column-direction wiring lines (14), insulating layers formed at intersections between the row-direction wiring lines and the column-direction wiring lines (Col. 7, lines 53-55), and a plurality of electron-emitting devices connected to the row-direction wiring lines (13) and the

column-direction wiring lines (14) (Col. 7, lines 22-25), and spacers (20) for maintaining an interval between the electron source (12) and the counter substrate (17) (Col. 8, line 65 to Col. 9, line 16 and Col. 27, lines 48-60) is electrically connected to the row-direction wiring lines (13) at different positions on the plurality of row-direction wiring lines (13) (Figure 2) characterized by comprising:

a circuit (external circuit or 1702) for sequentially turning on the plurality of row-direction wiring lines (13 or Dx through Dxm) (Figure 18 and Col. 19, lines 50-58); and

a controlled current application circuit (1707) for applying a predetermined controlled current to the plurality of column-direction wiring lines (14 or Dy through Dym) (Figure 18 and Col. 20, lines 46-59).

Regarding Claim 5, Mitsutake discloses that a section of the spacer (20) cut along a plane parallel to a plane (X) in which the counter substrate (17) spreads has a longitudinal direction in a direction in which the row-direction wiring line extends (See Figure 2 and Claim 16 of Mitsutake).

Regarding Claim 6, Mitsutake discloses that one of the spacers (20) is electrically connected to only one of the row-direction wiring lines (13 or $D_{x(m-1)}$) in Figure 2.

Regarding Claim 7, Mitsutake discloses that the spacer (20) comprises an insulating member (20a) as a spacer substrate and a semiconductor film (20b) as a portion formed from a material (Cu or Copper) having a resistivity lower than the spacer substrate (20a) (Col. 8, lines 63-65 and Col. 9, lines 18-43) since insulating member (20a), or spacer substrate comprises highly resistive or insulative material such as *glass* that insulates electrical conductivity between contacts and the semiconductor film (20a),

or the portion comprises conductive material such as *Copper* having much less resistivity to render *semi* electrical conduction.

Regarding Claims 8 and 9, Mitsutake discloses that an image forming apparatus comprises the electron source apparatus defined above, and an image forming member for forming member for forming an image by irradiation of electrons (electron beam) from the electron source apparatus (See Claim 26 of Mitsutake).

Remarks

The translation of the foreign provisional application is required for establishing foreign priority.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Shinoda (6,256,002) discloses a method for driving a plasma display panel comprising a step of applying the scan pulse sequentially to the second main electrodes.

Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Wilson Lee whose telephone number is (703) 306-3426.

Any inquiry of a general nature or relating to the status of this application should be directed to the Technology Center receptionist whose telephone number is (703) 308-0956.

Papers related to Technology Center 2800 applications may be submitted to Technology Center 2800 by facsimile transmission. Any transmission not to be considered an official response must be clearly marked "DRAFT". The Technology Center Fax number is (703) 308-7722 or (703) 308-7724.

Patent Examiner

WL

8/29/02